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IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE DIVISION

HYNIX SEMICONDUCTOR INC., HYNIX SEMICONDUCTOR AMERICA INC., HYNIX SEMICONDUCTOR U.K. LTD., and HYNIX SEMICONDUCTOR DEUTSCHLAND GmbH,

Plaintiffs,

v.

RAMBUS INC.,

Defendant.

No. CV-00-20905 RMW

ORDER ON HYNIX'S MOTIONS FOR JUDGMENT AS A MATTER OF LAW OR A NEW TRIAL REGARDING CLAIMS CONTAINING THE LIMITATION "DELAY LOCKED LOOP," "READ REQUEST," "ACCESS TIME REGISTER," OR "IN RESPONSE TO A RISING/FALLING EDGE"

[Re Docket Nos. 2068, 2069, 2070, and 2071]

Following the jury verdict rendered on April 24, 2006 in the patent trial in favor of defendant Rambus Inc. ("Rambus"), plaintiffs Hynix Semiconductor Inc., Hynix Semiconductor America Inc., Hynix Semiconductor U.K. Ltd., and Hynix Semiconductor Deutschland GmbH (collectively "Hynix") moved for judgment as a matter of law or, in the alternative, for a new trial on the issue of infringement of the claims containing any of the following limitations: "delay locked loop," "read request," "access time register," or "in response to a rising/falling edge." Rambus opposed the motions. The court has reviewed the papers and considered the arguments of counsel. For the reasons set forth below, the court denies Hynix's motions for judgment as a matter of law and, in the alternative, for a new trial.

I. BACKGROUND

Prior to the jury trial in this case, the court conducted a claim construction hearing. The court construed the disputed claim terms in a Claim Construction Order and accepted the parties' stipulated construction of certain other terms. *Hynix Semiconductor, Inc. v. Rambus Inc.*, 2004 WL 2610012 (N.D. Cal. Nov. 15, 2004). At trial, the jury was given the court's construction of the relevant terms and tasked with the responsibility of determining whether the limitations in the claims at issue are found in the accused products. The jury's verdict rendered on April 24, 2006 found infringement as alleged by Rambus. Hynix in the instant motion contends that the accused SDRAM and DDR SDRAM ("DDR") representative products do not literally satisfy the limitations which require: (1) a "delay locked loop" in claim 40 of U.S. Patent No. 6,426,916 (" '916 patent"), claim 34 of U.S. Patent No. 5,915,105 (" '105 patent"), and claim 33 of U.S. Patent No. 6,034,918 (" '918 patent"); (2) a "read request" in claims 24 and 33 of the '918 patent; (3) an "access time register" in claims 9, 28, and 40 of the '916 patent and claim 24 of the '918 patent; and (4) an output "in response to a rising/falling edge" transition of an external clock signal in claims 32 and 36 of U.S. Patent No. 6,378,020 (" '020 patent"). Hynix further contends that the "delay locked loop" and "read request" claim limitations are not infringed, as a matter of law, under the doctrine of equivalents.

The infringement questions raised in Hynix's current motion were the subject of pretrial summary judgment motions on infringement. The court issued the following orders on those motions:

Date & Docket No.	**Party Asserting Motion and Relief Sought**	**Limitation at Issue**	**Result**
5/12/2005 #1067	Hynix-non-infringement of "read request" under DOE	"read request"	Denied
5/12/2005 #1068	Rambus-literal infringement of "in response to a rising/falling edge"	"in response to a rising/falling edge"	Denied

2/24/2006 #1020	Rambus-literal infringement of "delay locked loop"	"delay locked loop"	Denied
3/17/2006 #1883	Rambus-literal infringement of "access time register"	"access time register"	Denied

The court now reviews the non-infringement contentions raised by Hynix's post-trial motions for judgment as a matter of law or, in the alternative, a new trial.

II. ANALYSIS

A. Legal Standards

1. Judgment as a Matter of Law

Under Rule 50(a) judgment as a matter of law is warranted where "a party has been fully heard on an issue and there is no legally sufficient evidentiary basis for a reasonable jury to find for that party on that issue." *Reeves v. Sanderson Plumbing Prods., Inc.*, 530 U.S. 133, 149 (2000). Judgment as a matter of law may be granted where "the evidence, construed in the light most favorable to the nonmoving party, permits only one reasonable conclusion, and that conclusion is contrary to that of the jury." *White v. Ford Motor Co.*, 312 F.3d 998, 1010 (9th Cir. 2002). A court reviews all the evidence in the record, but it disregards evidence favorable to the moving party that the jury is not required to believe:

> [I]n entertaining a motion for judgment as a matter of law, the court should review all of the evidence in the record. . . . [T]he court must draw all reasonable inferences in favor of the nonmoving party, and it may not make credibility determinations or weigh the evidence. Credibility determinations, the weighing of the evidence, and the drawing of legitimate inferences from the facts are jury functions, not those of a judge. Thus, although the court should review the record as a whole, it must disregard all evidence favorable to the moving party that the jury is not required to believe. That is, the court should give credence to the evidence favoring the nonmovant as well as that evidence supporting the moving party that is uncontradicted and unimpeached, at least to the extent that that evidence comes from disinterested witnesses.

Reeves, 530 U.S. at 150 (internal quotation marks and citations omitted).

2. Motion for a New Trial

A court may grant a new trial "for any of the reasons for which new trials have heretofore

been granted in actions at law in the courts of the United States." Fed. R. Civ. P. 59(a). In a motion for a new trial, the district court "can weigh the evidence and assess the credibility of witnesses, and need not view the evidence from the perspective most favorable to the prevailing party." *Landes Constr. Co. v. Royal Bank of Canada*, 833 F.2d 1365, 1371 (9th Cir. 1987). Even where the verdict is supported by substantial evidence, a new trial may be warranted if "the verdict is contrary to the clear weight of the evidence, or is based upon evidence which is false, or to prevent, in the sound discretion of the trial court, a miscarriage of justice." *United States v. 4.0 Acres of Land*, 175 F.3d 1133, 1139 (9th Cir. 1999). However, "a district court may not grant or deny a new trial merely because it would have arrived at a different verdict." *Id.* While there is no formulaic test for determining whether a verdict is contrary to the clear weight of the evidence, "[i]f, having given full respect to the jury's findings, the judge on the entire evidence is left with the definite and firm conviction that a mistake has been committed, it is to be expected that he will grant a new trial." *Landes Constr.*, 833 F.2d at 1372; *see also Koito Mfg. Co. v. Turn-Key-Tech, LLC*, 381 F.3d 1142, 1148-49 (Fed. Cir. 2004).

B. Delay Locked Loop

1. Claim Construction

The construction of patent claim terms is "exclusively within the province of the court." *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 372 (1996). Prior to trial the parties agreed to construction of the "delay locked loop" claim limitation as "circuitry on the device, including a variable delay line, that uses feedback to adjust the amount of delay of the variable delay line and to generate a signal having a controlled timing relationship relative to another signal." Joint Claim Construction and Prehearing Statement, *Hynix Semiconductor, Inc. v. Rambus Inc.*, C-00-20905, Docket No. 326, at 3 (N.D. Cal. Sept. 12, 2003) (hereinafter "Joint Statement"). A delay locked loop is also typically referred to as a "DLL."

2. Literal Infringement

For an accused product to literally infringe, it must be found to literally include each limitation called for in the claim, as construed. *Pall Corp. v. Micron Separations, Inc.*, 66 F.3d

1211,1217 (Fed. Cir. 1995). The application of the properly construed claim to the accused device involves a question of fact. *See Voice Technologies Group, Inc. v. VMC Systems, Inc.*, 164 F.3d 605, 612 (Fed. Cir. 1999).[1] Literal infringement requires a patentee, here Rambus, to prove by a preponderance of the evidence that every limitation of the asserted claim is literally met by the allegedly infringing device. *Enercon v. Int'l Trade Comm'n*, 151 F.3d 1376, 1384 (Fed. Cir. 1998).

At trial, Rambus offered as evidence the testimony of its expert, Robert J. Murphy, an electrical engineer, copies of the Hynix DDR data sheet, and copies of Hynix schematics of the DDR device. Murphy testified that a variable delay line "takes an input signal in, [ ] has some circuitry inside that creates a delay, and that delay is variable, or adjustable, via some control signal." Tr. Trans. 474:19-23. In other words, "we have an input signal coming in, some control signal which adjusts the amount of delay, then it drives another signal out." *Id.* 474:24-475:1. Turning to a schematic of the Hynix DDR, Murphy concluded that a "variable delay line" is present in the Hynix DDR device. He pointed out that (1) Hynix's schematic shows a box labeled "DLL," which contains a variable delay line; (2) the schematic below the box labeled "DLL" there is a signal line labeled as a feedback line; and (3) Hynix's lower level (more detailed) schematic shows circuitry containing a group of signals that control delay, an input signal, and an output signal, which together implement the variable delay line. *Id.* 477:17-479:14; 649:4-651:9.

Hynix argues that Rambus has not presented sufficient evidence to establish that the accused

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[1] Both parties treated the question of whether Hynix's DDR SDRAM product contains a "delay locked loop" as a factual question of infringement with Hynix asserting that Rambus offered no evidence that Hynix's product contains a "variable delay line." However, since there was no dispute as to the structure and function of Hynix's DDR SDRAM product, the issue may be more appropriately viewed as legal question of claim construction. *See MyMail, Ltd. v. America Online, Inc.*, 476 F.3d 1372, 1378 (Fed. Cir. 2007) ("Because there is no dispute regarding the operation of the accused systems, that issue reduces to a question of claim interpretation and is amenable to summary judgment."); *Rheox v. Entact, Inc.*, 276 F.3d 1319, 1324 (Fed. Cir. 2002) (where the parties do not dispute any relevant facts regarding the accused product but disagree over possible claim interpretations, the question of literal infringement collapses into claim construction and is amenable to summary judgment); *but see Int'l Rectifier Corp. v. IXYS Corp.*, 361 F.3d 1363, 1375 (Fed. Cir. 2004). Nevertheless, since the parties stipulated to the interpretation of "delay locked loop" and Hynix has framed the issue as whether there was a legally sufficient basis for the jury to find for Rambus, the court reviews the question on that basis.

Hynix DDR device[2] includes a delay locked loop as construed. Specifically, Hynix contends that it is uncontroverted that the DDR device implements variable delay using an entire circuit with a series of fixed delay elements while "delay locked loop," as construed, describes a single line or path containing individual variable delay elements that are voltage controlled to vary delay. Hynix's interpretation of the parties' agreed upon construction of delay locked loop is too narrow. The construction does not require a single path on which the voltage is controlled as opposed to an electrical path on which delay is controlled by the selection of fixed circuits connected to the path.

The jury's verdict that Hynix's DDR SDRAM meets the delay locked loop limitation is supported by substantial evidence. The verdict is also not contrary to the clear weight of the evidence.

C. Read Request

1. Claim Construction

The parties accepted the Federal Circuit's construction in *Rambus Inc. v. Infineon Techs. AG*, 318 F.3d 1081, 1093 (Fed. Cir. 2003) of "read request" as "a series of bits used to request a read of data from a memory device where the request identifies what type of read to perform." Joint Statement, at 1.

2. Literal Infringement

The parties do not dispute that "read" and "read with autoprecharge" both consist of a series of bits that define commands in the Hynix device. Hynix submits that the evidence presented by Rambus does not show that the Hynix device uses a read command that "identifies what type of read to perform." Rambus asserts, as it did at trial, that these two commands—"read" and "read with autoprecharge"—constitute two different types of read commands. Hynix responds that the output data is the same whether the command is "read" or "read with autoprecharge" so there cannot be two "types" of read commands. Hynix emphasizes that the autoprecharge command does not serve to

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[2] Hynix's memorandum of points and authorities in support of its motion fails to make clear that only the DDR device has been accused of infringing claims containing the delay locked loop limitation.

identify the "type of read," but rather serves the separate function of setting up the sense amplifiers for the next read. Rambus does not dispute that the output from the two commands is the same but points out that Hynix offers nothing other than its argument which suggests that "reads" must be distinguished based upon differences in output data as opposed to some other difference, "such as the series of bits used to specify the read, or the state of the sense amplifiers following a particular read." Rambus Opp'n at 4:5-7. The issue thus boils down to whether "read" and "read with autoprecharge" each constitute "a series of bits used to request a read . . . where the request identifies what type of read to perform."[3]

At trial, Rambus's expert witness, Murphy, testified that the Hynix devices performed four types of reads: (1) a read without autoprecharge, (2) a read with autoprecharge; (3) a normal mode read; and (4) a page mode read. Tr. Trans. 433:20-434:1. He acknowledged, however, that "the normal mode read is essentially . . . similar to a read with autoprecharge. . . . And a page mode read is similar to a read without autoprecharge." *Id.* 434:7-11. Murphy elaborated that the distinction is that a "read with autoprecharge" causes the sense amplifiers to set up the next read with precharge while a "read" alone does not set up the next read. *Id.* 623:11-19. Changing the value of the A10-bit differentiates the "read" and "read with autoprecharge" commands. *Id.* 434:12-435:20 citing to Trial Ex. 5060 (SDRAM datasheet) at 12 and Trial Ex. 5011 (SDRAM timing diagram) at 15; Trial Tr. 436:11-438:10 citing to Trial Ex. 5064 (DDR SDRAM data sheet) at 10, 51-52. The A10-bit is always decoded no matter what type of read is performed and is not separable from the read

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[3] The parties frame the issue as whether "read" and "read with an autoprecharge" are different "types" of reads, in other words, does the fact that the output of data following a "read with autoprecharge" command and that following a "read" command is the same preclude a finding that Hynix's method includes two types of reads? Although the parties did not ask the court to define "read" or what constitutes a "type of read," the qestion of what constitutes of a"read" or "type of read" is probably more properly viewed as a claim construction issue than as a factual question of infringement. *See MyMail*, 476 F.3d at 1378; *Rheox*, 276 F.3d at 1324; *but see Int'l Rectifier*, 361 F.3d at 1375. However, since the parties stipulated to the interpretation of "read request" and Hynix has framed the issue as whether there was a legally sufficient basis for the jury to find for Rambus, the court reviews the question on that basis. The court, however, also concludes that a proper construction of claims 24 and 33 of the '918 patent does not mean that for there to be a different "type" of read request, there must be different output of data. *See Rambus Inc. v. Hynix Semiconductor, Inc.*, 2008 WL 5047924, *11-*12 (N.D. Cal. Nov. 24, 2008) (holding that a write and write with autoprecharge constitute different "types" of write request).

commands. Trial Tr. at 2709:25-2712:18.

Murphy also noted that a "read" command permits the interim issuance of a "burst terminate" command to interrupt the data coming out of the device before the completion of the read request. Tr. Trans. 619:7-20. Murphy distinguished this from a "read with autoprecharge," which does not permit the data coming out of the device to be interrupted by a later issued "burst terminate" command. *Id.* 619:21-24.

Hynix's expert, David L. Taylor, also an electrical engineer, opined that in order for there to be different types of read commands, there must be a difference in the data output by the read command. However, Taylor also testified that "precharge is a very different type of operation inside of a DRAM part." Tr. Trans. 1624:1-2. Taylor explained that the autoprecharge is a command that directs the part to perform a function after it completes the read command. *Id.* 1626:14-22. Thus, where there is a "read with autoprecharge" the device performs the read request and then precharges "to get ready for the subsequent read."

The evidence supports the conclusion that Hynix's SDRAM and DDR SDRAM products perform two "types" of reads. The read request limitation does not require that the output of data be different. The autoprecharge affects the way in which a read is accomplished. The fact that the output may be the same from a read without autoprecharge and a read with autoprecharge does not mean the reads are of the same "type." *Accord Infineon*, 318 F.3d at 1093 (distinguishing normal-mode and page-mode "types" of access); *Rambus Inc. v. Hynix Semiconductor, Inc.*, 2008 WL 5047924, *11-*12 (N.D. Cal. Nov. 24, 2008) (holding that a write and write with autoprecharge constitute different "types" of write request).

D. Access Time Register

Hynix moves for judgment as a matter of law that it does not infringe any claim containing an "access time register" limitation. Hynix argues that the parties do not dispute the facts regarding the accused devices' operation, and that the dispute reduces to a matter of claim construction for the court. *See MyMail*, 476 F.3d at 1378; *Rheox*, 276 F.3d at 1324; *General Mills, Inc. v. Hunt-Wesson, Inc.*, 103 F.3d 978, 983 (Fed. Cir.1997).

1. The CAS Latency Value in Hynix's SDRAM and DDR SDRAM

The SDRAM contains a programmable mode register. Tr. Trans. 450:7-14. When the mode register is programmed, address pins A4, A5, and A6 determine a value called CAS latency. *Id.* at 450:15-22. The CAS latency equals the amount of time that transpires between the DRAM receiving a read command and the data being available. *See id.* at 692:12-17; 462:23-463:1; 711:24-712:4. The SDRAM can accommodate CAS latency values of 1, 2, or 3. *See id.* at 450:20-22. The DDR SDRAM has a similar mode register, but can accommodate a different range of programmable CAS latency values. *Id.* at 452:21-453:16.

It is fundamental to note that CAS latency does not *equal* the amount of time before the DRAM begins outputting data. *See id.* at 713:3-19. The CAS latency equals the amount of time before the data is available on the bus's data lines. *See id.* To make that data available, the DRAM must begin to output data before the CAS latency period expires. *See id.* For example, in an SDRAM programmed with a CAS latency of 2, the DRAM cannot output data in response to a read request until one clock cycle transpires. *Id.* at 713:12-18; 2004:24-2005:5. Similarly, an SDRAM with a CAS latency of 3 cannot output data until two clock cycles have transpired. *See id.* at 713:19-714:2; 2005:15-19. Once one or two clock cycles have occurred, the data must be output within a time t_{AC}. *Id.* at 2004:15-23. The value t_{AC} is a parameter of the SDRAM that defines the maximum amount of time it takes for the device to output data. *Id.*; *see id.* at 459:14-462:9; 1644:7-1645:2.[4] In other words, the Hynix SDRAM outputs data at some point within the window of time between:

$$\text{CAS latency} - 1 \quad \text{and} \quad \text{CAS latency} - 1 + t_{AC}$$

By outputting data within this window, the SDRAM ensures that the data will be available to be read after the CAS latency period has transpired.

The DDR SDRAM operates similarly. Because the "double data rate" SDRAM can use both

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[4] In the Hynix SDRAM, the t_{AC} value varies from as little as zero to a maximum of 5.4 or 6 nanoseconds (depending on the CAS latency). Tr. Ex. 5060 at 7; Tr. Trans. 466:22-467:13. To put this parameter in context, the Hynix SDRAM operates at frequencies on the order of 100 to 166 MHz. Tr. Ex. 5060 at 1. This implies that one clock cycle lasts about 6 to 10 nanoseconds and further implies that the access time t_{AC} (at its maximum) may consume nearly an entire clock cycle at the SDRAM's highest operating frequencies.

edges of the clock signal, it permits CAS latency values of 2 and 2.5 clock cycles. *See* Tr. Ex. 5064 at 3 (listing features); 20 (demonstrating mode register programming for different CAS latency values). The DRAM begins to output data in response to a read request after 1.5 and 2 clock cycles respectively. Tr. Trans. 463:20-466:21. The precise timing of the output depends again on the access time t_{AC}. *Id.* 466:14-467:18. There is, however, a "small difference"[5] in the DDR SDRAM in that t_{AC} (which the data sheet formally defines as the "data-out edge to clock edge skew") can be negative; it ranges from -0.75 nanoseconds to +0.75 nanoseconds. *Id.* 467:4-13; Tr. Ex. 5064 at 41. This does not meaningfully change the data output window from that in the SDRAM. In Hynix's DDR SDRAM, data output occurs between:

$$\text{CAS latency} - 1 - |t_{AC}| \quad \text{and} \quad \text{CAS latency} - 1 + |t_{AC}|$$

In other words, data output occurs after 1.5 or 2 clock cycles, ± 0.75 nanoseconds.

2. The Asserted Claims and Their Construction

Four of the asserted claims contain what the parties refer to as an "access time register" limitation. The "access time register" limitation appears in three variations:

"receiving a value that is representative of a number of cycles of an external clock signal to transpire after which the memory device responds to a first operation code"	"a register which stores a value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data"	"storing a delay time code in an access time register, the delay time code being representative of a number of clock cycles to transpire before data is output onto the bus after receipt of a read request and wherein the first amount of data corresponding to the first block size information is output in accordance with the delay time code"
U.S. Patent No. 6,426,916 (claim 9).	U.S. Patent No. 6,426,916 (claims 28, 40).	U.S. Patent No. 6,034,918 (claim 24).

The court's claim construction order addressed these limitations jointly and construed them in light of each other. *Hynix*, 2004 WL 2610012, *16-*20. The court construed "access time register" ('918 claim 34) as "a data storage element to store a value representative of a time a device

[5] The "small difference" is likely due to the DDR SDRAM's use of a separate strobe to control data input and output timing. *See* Tr. Ex. 5064 at 3; *see also Rambus*, 2008 WL 5047924, *16-*19.

must wait from receiving a transaction request before responding to a transaction request." *Id.* at *19. The court construed "a value that is representative of an amount of time to transpire" ('916 claims 28 and 40) as "information that indicates an amount of time which is to occur." The court also construed "value which is (or code being) representative (or indicative) of a (preprogrammed) number of clock cycles" (all claims) as "information which indicates a number of clock cycles." The court explained that the value represents a time delay, and that the boundaries of the delay period are further defined by the specific claim language:

> [T]he court uses the phrase "receiving a transaction request" to describe the starting point of this time delay. To the extent this phrase contains any ambiguity, the court notes that the claims using "access time register" often describe the starting and ending events used to measure this delay time code. The court intends for its construction to be interpreted as a generic term which is further defined by the specific claims at issue.

Id. at *18 n.19.

Those constructions aside, the true dispute between Rambus and Hynix turns on the meaning of "representative." As explained above, the CAS latency value does not *equal* the amount of time that transpires before the DRAM outputs data in response to a read request. The CAS latency values equals the amount of time until the data is available to be read by the memory controller. A Hynix engineer, Jae Jin Lee explained the concept the clearest (despite his need for a translator): "The fact is when it comes to latency, that is really not to be looked at from the perspective of how long one must wait before there's data, but rather from a system perspective with respect to the data that is required, the point is when such data is made available, that is the crux of the point." Tr. Trans. 711:12-18.

To Hynix, the fact that the CAS latency value is greater than (and not equal to) the amount of time that must transpire before the DRAM outputs data is fatal to Rambus's infringement claims. Rambus accepts that the CAS latency value does not equal the amount of time that must transpire before the DRAM outputs data. But Rambus urges that the CAS latency value does *represent* or *indicate* the amount of time that must transpire before the DRAM outputs data.

Hynix's interpretation is too narrow. Rambus's claims do not require that the stored value

equal the amount of time before the device outputs data. On the contrary, the claims explicitly cover stored values that are *representative of* the amount of time before the device outputs data. As discussed above, the stored CAS latency value equals the amount of time until the data is available to other devices. To meet the "goal" of having data available after the latency period, the CAS latency value dictates the DRAM's responses to a read request. The DRAM begins to output data after a period of time that is a function of the CAS latency value (and a constant, t_{AC}, that depends on the device's conditions and quality). Given this direct functional relationship between the CAS latency value and when the device outputs data, the court agrees with the jury that the CAS latency value "is representative of" the amount of time before the device begins to output data.

E. In Response to a Rising (or Falling) Edge Transition

1. Claim Construction

The "in response to the rising (or falling) edge transition" limitation appears in asserted dependent claims 32 and 36 of the '020 patent incorporated from independent claim 30. The parties stipulated that the limitation means "as a result of a transition of the external clock signal from a lower (higher) voltage level to a higher (lower) voltage level." Joint Statement at 5; Tr. Trans. 468:2-17.

2. Literal Infringement

Hynix appears to advance three arguments for why it is entitled to judgment as a matter of law. It first argues that Rambus failed to introduce sufficient proof of infringement. It next argues that the DDR SDRAM's use of a complementary clock cannot infringe this limitation. Finally, it appears to argue that the DDR SDRAM does not output data in response to the clock's transitions, but in response to internal timing pulses. None of the arguments has merit, and the court denies the motion.

First, Hynix argues that there is no evidence that the DDR SDRAM possesses this limitation because Murphy never testified that the device outputs data "as a result of" a rising or falling edge transition. Hynix's argument takes a "magic words" approach to infringement that has no basis. It appears true that Murphy never used the words "as a result of" in his testimony. But he did say the

following:

- [explaining a timing diagram] We have a clock signal and its opposite, clock bar. So when this one is low, this one is high. When this one transitions from a low to a high, its opposite transitions from a high to a low. Those transitioning wave forms give rise to a crossing point at the center. Then we go a half clock cycle later and the clock falls from a high to a low and clock bar rises from a low to a high, causing another crossing point. Data from these devices is output from the device nominally coincident with this point in time. Tr. Trans. 470:1-14.

- [explaining the same diagram] So we can see that both for the rising edge of clock and the falling edge of clock, data is output synchronously with respect to the clock. Tr. Trans. 471:1-3.

- You must have rising and falling transitions to make the data be output from the device. Tr. Trans. 471:12-14.

- [referring back to the diagram] And outputting a first portion of data in response to a rising edge transition of the external clock signal, I explained external clock signals and how they are received by the Hynix DDR SDRAM device, and you remember this board over here where I showed that the output data comes out in response to a rising edge transition; and in the second paragraph here, it also comes out in response to a falling edge transition. Tr. Trans. 499:7-15.

- But the thing is -- there's a causal relationship between the clock switching here and the output being sent out of the part and that's exactly what this block diagram shows one of ordinary skill in the art, that there's a cause and effect between the clock and the clock bar and the DLL block and the clock under DLL signal and the output buffers. Tr. Trans. 2722:14-21.

In light of this testimony, Rambus presented sufficient evidence for the jury to find that the DDR device outputs data "as a result of" a rising or falling edge transition.[6]

Hynix's second argument is the device does not output data in response to *a* transition of the external clock signal. This occurs because the DDR SDRAM outputs data as a result of the crossing of two clock signals, CLK and its complement CLK/.[7] *See id.* 470:1-11; 1677:23-1678:24. Hynix argues that "[t]he fact that no crossing point can be made without a rising edge of one clock and the

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[6] Rambus also argues in its opposition that "Mr. Lee testified that data in the Hynix DDR SDRAM device is referenced to the rising edge and falling edge of an external clock signal, as indicated in the Hynix DDR SDRAM data sheet, consistent with Mr. Murphy's opinion and the jury's verdict of infringement." Opp'n at 4 (citing Tr. Trans. 784:3–785:21). Rambus's characterization of Mr. Lee's testimony is mistaken. He testified that *address* and *control* signals are latched to the rising and falling edges of the clock. Tr. Trans. 784:3–785:21. The cited testimony does not discuss data signals.

[7] Taylor testimony also referred to CLK/ as "CLKZ." *See* Tr. Trans. 1677:23-1678:21. For simplicity the two clock signals will be referred to as CLK and CLK/ in this order.

falling edge of the other (and vice versa) is simply irrelevant." Mot. at 7. On the contrary, this fact is precisely why Hynix's device infringes this limitation. Rambus's claims cover devices that output data as a result of a rising or falling edge of a clock signal. The DDR SDRAM outputs data as a result of two things: a rising edge of one clock signal and the falling edge of its complement. To be sure, Hynix has added something to Rambus's claimed invention. But "[i]t is fundamental that one cannot avoid infringement merely by adding elements if each element recited in the claims is found in the accused device." *Stiftung v. Renishaw PLC*, 945 F.2d 1173, 1178 (Fed. Cir. 1991) (quoting *A.B. Dick Co. v. Burroughs Corp.*, 713 F.2d 700, 703 (Fed. Cir. 1983)).

Perhaps Hynix means to argue that Rambus's claims must be limited to devices employing only a single clock signal, and that the use of two clock signals to output data pulls Hynix's device outside the literal scope of the claim. Nothing in the patent suggests such a narrow reading of the claims. The invention does not turn on minimizing the number of clock signals needed (which might have supported reading in a ceiling to the number of clock signals). With no reason to limit the claim to devices employing precisely one clock signal, the court cannot accept Hynix's argument.

Finally, Hynix appears to argue (largely in its reply) that its DDR SDRAM cannot infringe as a matter of law because the device outputs data as a result of an "internal timing pulse," not the rising or falling edge of the external clock signals. This argument also fails. The testimony at trial established that the crossing point of the clock signals trigger the "internal timing pulses" that directly cause the device to output data. Tr. Trans. 2721:6-2722:21. Again, nothing in the patent narrows the claim to cover the output of data *directly* in response to the transition of the clock signal. Though the connection between the clock signal transition and the "internal timing pulse" is indirect, it does not sever the causative relationship between the transition of the clock signal and the output of data that is covered by this limitation of Rambus's claims.

III. ORDER

For the foregoing reasons, the court denies Hynix's motions for judgment as a matter of law of non-infringement with respect to the asserted claims containing the "delay locked loop"

limitation, the "read request" limitation, the "access time register" limitation, and the "in response to a rising/falling edge" limitation. The alternative motion for a new trial is also denied.

DATED: 12/2/2008

Ronald M. Whyte

RONALD M. WHYTE
United States District Judge

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C-00-20905.

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